Fabrication of Amorphous Metal Oxides Thin Film Transistor Using Custom Designed Spin Spray Pyrolysis Unit

Synopsis submitted in fulfillment of the requirements for the degree of

Doctor of Philosophy

in Electronics

by

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Synopsis of the Doctoral Thesis

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1.1 Introduction

Microelectronic is a study of the manufacturing of minute electronics design and components. These components are made up of semiconductor materials. These components may include active or passive components. Some of the active components are diodes and transistors, whereas the basic passive components are resistors, capacitors, and inductors.

Microelectronic technology includes thin film, thick film, hybrid, integrated circuits, or a combination of all the above. Such circuits are applied in digital, switching and linear circuits. Every microelectronic circuit is composed of logic or memory, or a combination of both.

The basic building block of any microelectronic circuits is a transistor. The transistor is a three-terminal electronic device that acts as a switch. There are many different kinds of transistors such as bipolar junction transistors (BJT), field-effect transistors (FET), Junction field-effect transistors, metal oxide semiconductors field-effect transistors (MOSFET) and thin film transistor (TFT)[1]. Currently, most of the industries are using MOSFET for microelectronic circuits, mainly silicon-based MOSFET. But due to the fabrication complexity and cost of both equipment and silicon wafers, the researchers are trying to look for alternative technology that reduces the use of silicon wafers and the simplicity and expense of the equipment.

Many numbers of research groups have been working on group II-VI based semiconductor materials and organic semiconductors, an alternative to silicon-based materials. Among them, the oxide semiconductor is extensively studied like IGZO [2], SnO_2 [3], IZO [4], GZO [5], and ZnO [6]. Pentacene [7], polyaniline [8], polypyrroles, polythiophenes, and polyphenylenevinylenes are organic semiconductor materials[9]. The oxide semiconductor has gained attention due to numerous merits like transparency [10], low temperature [11], excellent chemical stability, higher mobility, and process versatility [12]. Group II-VI based semiconductor materials can be deposited as thin films by using the vacuum and non-vacuum techniques.

In contrast, organic semiconductor materials are deposited only by non-vacuum techniques. Some of the vacuum techniques are thermal evaporation[13], sputtering, atomic layer deposition (ALD)[14], pulsed laser deposition (PLD), and chemical vapor deposition (CVD)[15]. The vacuum techniques have advantages in films deposited such as uniform, accurate, and non-contaminated, but this technique require high temperatures and complexity in processing. They are also very expensive to install in each research institution. Drop-casting, Doctor blade, Dip coating, spin coating, and spray coating are a non-vacuum process that is economical compared with the vacuum process. Still, thin films fabricated using these techniques are non-uniform in thickness and may be affected by contamination defects. In Drop-casting, Dip coating, and spin coating processes are difficult to use a shadow mask technique to fabricate different configurations. The existing spray coating unit is a simple, economical, low-temperature coating process and can form different structures using shadow masks, but the resulting films are often non-uniform.

The technique stated earlier are suitable for thin film are deposition[16]. The deposited thin films are used for the fabrication of TFTs as an active layer. The TFT is a kind of field-effect transistor (FET)[17]. Its construction and operation principles are similar to those of the metal oxide field-effect transistor (MOSFET), which is the crucial device element in modern integrated circuits (ICs). The progress histories of TFTs and MOSFETs are similar. The TFTs are classified into three depending on the semiconductor material used for an active layer, namely organic, inorganic, and hybrid.

The construction of TFTs consists of electrodes and dielectrics in addition to active materials. The dielectric materials are also known as gate insulators. The most commonly used gate insulator in industries is SiO_2. The SiO_2 has very low leakage current and high break down voltage, but as a counterpart, the deposition of SiO_2 is at high temperature, complicated and expensive process. Thus, there is a requirement for alternative materials for gate dielectrics in the case of TFT fabrication. Research groups are working on Y_2O_3, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, and TiO_2 [18] [19] [20]. Although these are excellent dielectric

materials, they are deposited at a higher temperature. Hence, the use of these metal oxide dielectrics cannot be used for flexible electronics. Consequently, dielectrics are gaining more attention. The major dielectrics are PVP, PVA, cellulose acetate, and PDMS [21].

The TFTs are fabricated on glass, silicon, PET, paper, OHP sheet, Teflon, and kepton. Among them, glass, PET, and silicon are nonflexible. Flexible substrate-based TFTs are vital devices for future wearable electronics systems.

Organic and printed electronics is focused on integrating new materials with cost-effective, large-scale manufacturing processes that open up new technology fields. Thinness, light weight, versatility, and protection of the environment are the main benefits of organic electronics. Organic electronics also allows the development and direct integration of a wide range of electrical components.

Many research groups have been fabricating the TFTs using the vacuum or by solution-processed technique. In vacuum techniques, there are many methods, such as thermal evaporation, sputtering, ALD, PLD, CVD, etc. These methods have some bottleneck, such as material choice for coating, temperature for coating, cost of the equipment, and scalability to the industry's needs. In the solution-processed technique, the primary methods are drop-casting, Doctor Blade, Dip coating, spin coating, spray coating, the bottleneck in these methods are masking and uniformity in the coating.

To overcome the above mentioned problems, we have built a new system. The system allows to use solution-processed techniques and it is scalable to industrial needs. The system enables to decrease the deposition temperature and it give freedom to select materials for deposition. However, it is an economical process.

The major problem of next-generation TFTs is the fabrication on flexible substrates for wearable electronics. Construction of TFTs on a flexible substrate, many groups of researchers is looking for materials that can be deposited at a lower temperature. Some of the materials that can be deposited at a lower temperature are polyaniline, pentacene, a-ZnO, a-IZO, a-GZO, and a-IGZO [22].

Among them, Indium and gallium are rear earth metals, which are very expensive. The a-ZnO has good mobility, stability, environment-friendly, and low cost. PANI also has advantages over other organic active materials. Some of the advantages of PANI are biodegradability, cost-effective, and non-corrosive[23].

The following problems are identified based on the literature review. The identified problems can be divided broadly into two major categories namely design, development, and optimization of spin-spray pyrolysis (SSP) and fabrication of TFTs using inorganic, organic and hybrid materials as active layers on glass and flexible substrates for universal logic gate applications

The first part is focused on the design and development of customized spin-spray pyrolysis unit for uniform film deposition at low temperatures in simple and economic systems. The system is optimized for PANI, PANI / ZnO hybrid nanocomposite, and ZnO thin film deposition.

The second part is the fabrication of PANI, PANI / ZnO hybrid nanocomposite, and ZnO material based TFTs. Further inverter, NAND gate, and NOR gate were fabricated and characterized using these TFTs.

Objective

- Design and construction of spin-spray pyrolysis (SSP) unit.
- Synthesis, deposition, and optimization of thin film transistor layers
    - PVA by drop cast method.
    - PANI, PANI / ZnO hybrid nanocomposite (NC) by SSP unit.
    - ZnO using the SSP unit.
- Deposited thin film transistor layers are characterized.
- Fabrication of thin film transistor using PANI, PANI / ZnO hybrid NC, and ZnO.
- Thin film transistor fabricated is electrically characterized.
- Universal gate (NOT, NAND, NOR) is implemented of fabricated TFTs.

1.2 Thesis Organization

The thesis focuses on the fabrication of amorphous metal oxide thin film transistor using a custom-designed spin spray pyrolysis unit. The thesis is structured into seven-chapter. The flow is explained in each chapter.

Chapter 1; Introduction: Briefly describes the history of the microelectronic system with the essential element called transistor. The materials used for making a thin film transistor. Based on the literature review identified and defined the problem in the development of TFT. The aim and scope of the thesis are outlined in this chapter.

Chapter 2; Thin Film Transistor: The history of the TFT is studied. Discussion are made on the development of TFT. The different architecture of TFT is explained along with the principle of operation. The classification of TFT depending on the active material used. The introduction to the classified active layer materials planned.

Chapter 3; Experimental methods: In this chapter, we discuss the deposition process of thin films such as oxide semiconductors, gate dielectrics, and metal contacts for TFTs. We also studied different characterization techniques for materials used for fabrication.

Chapter 4; Design and construction of spin spray pyrolysis: We discuss the design and development of the spin spray pyrolysis unit. The specification and significance of the components used for construction are discussed in detail. The working principle and operation of the system are explained. The merits and novelty of the system have discoursed. The system is tested for different coating materials and also by varying the parameters of the system.

The spin-spray pyrolysis unit is designed and developed as shown in Figure 1 using the components with the desired specifications as given in *Table* 1.

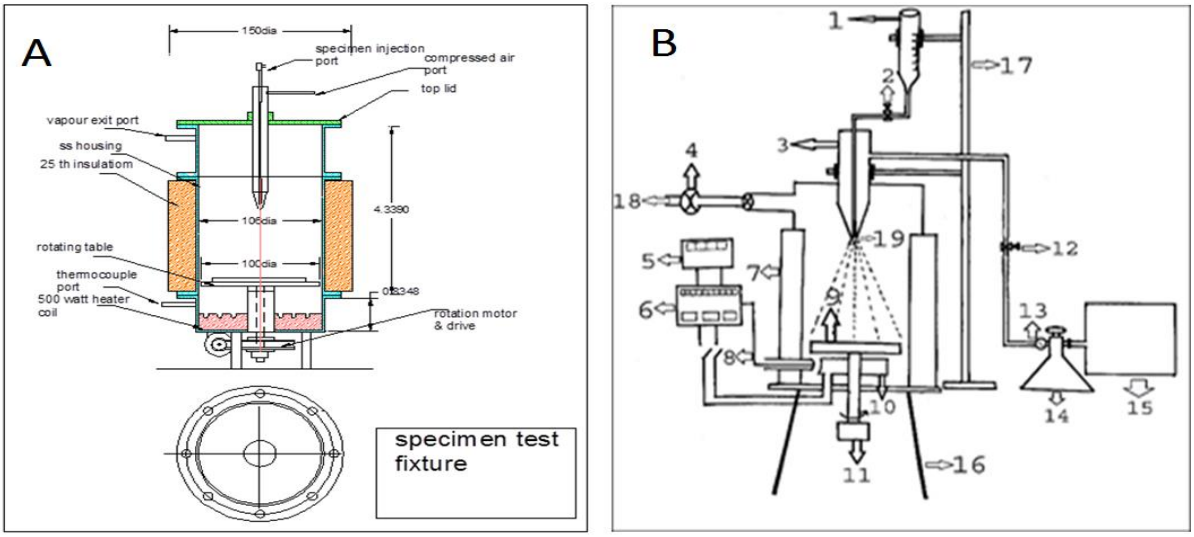


Figure 1 Schematic Diagram of Spin Spray Pyrolysis (A AutoCAD Design, B Manual Design)

Table 1 Specifications and lists of SSP components

No.	Name	Specification	Function
1	Burette	Volume = 0.1-15 ml	Solution storage tank
2	Solution feeder valve	Flow rate = 1-5 ml/min	Allows to vary the flow rate
3	Sprayer	Material= Quartz	For atomization of solution.
4	Exhaust fan	Size=120X120X38 mm Speed=2600-2800 rpm Airflow = 95-105 CFM	Avoid catching fire due to the presence of alcohol in the solution.
5	Temperature display	Delta make	The temperature display unit consists of a switch and knob to set the temperature
6	Temperature controller unit	Relay controller	Helps to maintain the temperature
7	Chamber	Material = SS314, Al sheet Inner diameter = 150mm Outer diameter = 204 mm	The housing of inner components, Maintain the temperature in the chamber
8	Thermocouple	Type = K-type Max temp = 1000℃	Used to measure the temperature of the substrate.
9	Substrate holder	substrate size <100mm	To hold multiple substrates.
10	Heater	Max = 450℃	Heating the substrate.
11	Substrate rotator	Speed = 50-100 rpm	For uniform coating.
12	Air control valve		Maintain pressure.
13	Pressure gauge	0-7 bar	To measure the pressure.
14	Air cylinder	5lts	To store the compressed air.

15	Compressor pump	0.5HP 3lts/m	To provide air at 1bar.
16	Equipment stand	20 Cm	To provide stability to equipment.
17	Burette holder		To hold the burette and the sprayer.
18	Air exhaust	Material = PVC pipe and other connectors	To pull out the air.
19	Spray nozzle	Inner diameter= 0.3mm	An area where the pressure difference is created.

Merits of the Spin Spray Pyrolysis Unit

The spin spray pyrolysis unit is a simple and quick method for the deposit of metal oxide, CNT, polymers thin films. It is one of the best choices for deposition of low cost, large area scalable thin films. The system is capable of utilizing material effective for thin film deposition. The system is equipped with the rotation mechanism to avoid the movement of the sprayer, which is not available in the existing system.

When compared to the existing system, a nozzle can be used instead of an ultrasonic atomizer. The diameter of the spray drops is governed by the size of the nozzle head, the surface tension of the precursor solution, its viscosity and the pressure difference before and after the spraying. Alternatively, ultrafine dispersive powders could be produced by the swift rise of the temperature in-side the chamber.

The rotation enables uniform film deposition throughout the area. The weight and size of the system are lighter and smaller. The system can be assembled and disassembled at any point in time, which makes it easy to handle and portable. The system is fabricated with the cost of 60,000/- in Indian Rupees (INR), which is lower than the existing systems which are not less than 10,00,000/- INR.The developed system weights 25kgs which is composed of different components with their specifications as revealed in *Table* 1. The total cost of the system is around 60000/- INR which is the lowest in the market. The system can be assembled and disassembled whenever required. As a result, it is portable. Another unique feature of the system is it is capable of rotation of the

substrate. Using the system, we have deposited thin films of different materials at the various temperature on dissimilar substrates.

Results

The results of the experiments are tabulated as reviled in Table *2*. In addition, we have optimized the system for coating ZnO thin-films for various thickness. The ZnO thin-films were used for fabrication the thin film transistor for microelectronics application.

Table 2 Deposition of different thin film on various Substrate.

No.	Sample	Substrate	Temp (℃)	Morphology	Optical
1	ZnO	Glass	150	Formless	Milky
			170	Formless	Milky
			200	Nanoflakes	Translucent
			250	Nanoleaf	Translucent
			275	Nanodisc	Transparent
			300	Nanoworm	Transparent
		Teflon	250	Nanoleaf	Transparent
2	CNT	FTO coated glass	100	Nanotubes	Opaque
3	GZO	Glass	250	Nanodisc	Translucent
4	PANI	Glass	75		Green
5	PANI/ZnO hybrid	Glass	75		Dark Green

Chapter 5; Synthesis characterization and application of PANI and PANI doped ZnO based TFT: In this chapter, we review the literature on the organic semiconductor material. The deposition of PANI and PAN-ZnO thin films using different methods on the OHP sheet and glass substrate. These thin films are examined for various properties related to materials. The films are used for the fabrication of TFT. The characteristics of TFT are studied and compared. PANI/ZnO is TFT that is used for construction and testing of logic gates.

PANI thin films: The thickness of the thin film is in the range of 400nm. The roughness of the samples is between 16-17 nm. The resistance of the films is 90MΩ. The morphology shows the films uniformity.

PANI/ZnO hybrid thin films: The thickness of the thin film is in the range of 600nm. The roughness of the samples is between 17-19 nm. The resistance of the films is 1MΩ. The morphology shows the films uniformity.

PVA film: The thickness is about 600 nm. It exhibits a maximum transmission of 90% at 550nm and the sharp ultraviolet edge is seen at 290 nm. The energy band gap is found to be 3.9 eV. The dielectric constant (Ɛr) of the film is found to be 8 at 40 Hz.

Fabrication and Characterization of PANI based TFT

Fabrication of PANI based TFT on OHP Sheet:. The OHP sheet is kept on a hot plate and heated to 75℃. The PANI solution id drop-cast on to the heated substrate. The silver ink is coated and used as electrodes to TFT. The PANI and OHP sheet acts as semiconductor and insulator material for the TFT. The silver paste act as a source, drain and gate electrode. The W/L ratio of the TFT is 2000/500 µm, as shown in Figure 2.

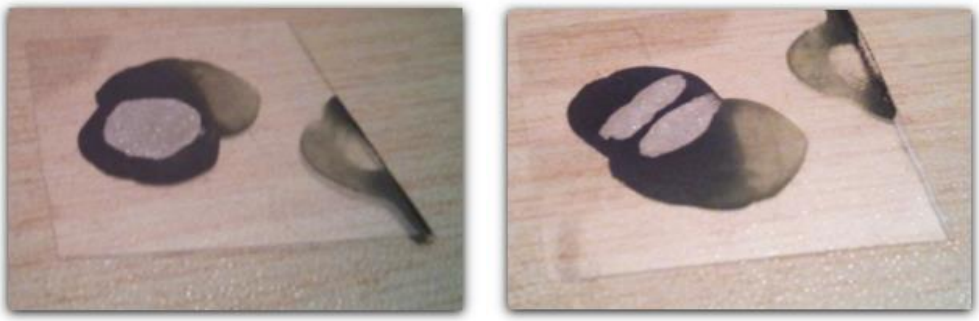


Figure 2 PANI based TFT as-fabricated on OHP sheet

Characterization of TFT on OHP sheet: The Fabricated TFT is tested for its input and output characteristics. The threshold voltage (Vth) is determined tobe 4.5 V, as shown in Figure 3. The Ion/off is in the range of 10^1as show n in Figure 3.

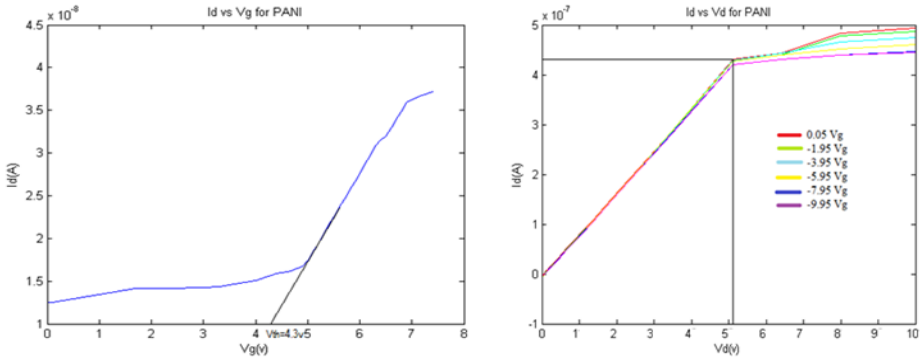


Figure 3 Input and Output Characteristics PANI based TFT on OHP

Fabrication of TFT on Glass: Top Gate-Top contact transistor is fabricated on the glass which is pre-coated with aluminium as a source and drain electrodes, PANI and PVA all using custom-designed masks. The PANI acts as an active layer and PVA acts as a gate dielectric for the fabricated TFT. The Fabricated TFT is as shown in Figure 4

Figure 4 PANI based TFT as-fabricated

Characterization of TFT on Glass: The Fabricated TFT is tested for its input and output characteristics. The Vth is determined to be 3.2V, as shown in Figure 5. The value of μ_{lin} is found to be 2.8X10^{-4} cm/Vs. The Ion/off is in the range of 10^2 as shown in Figure 5.

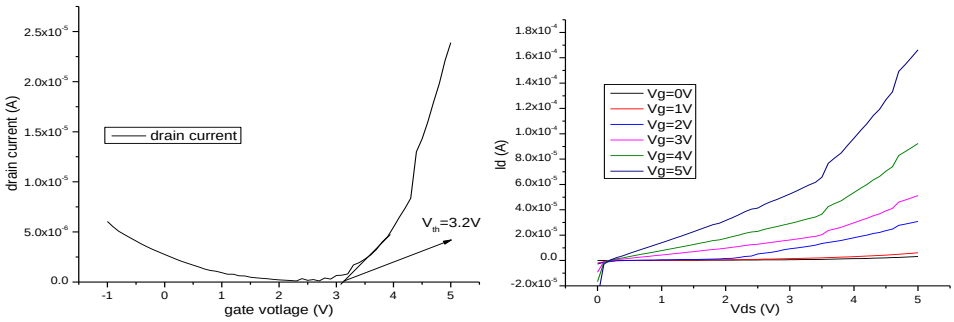


Figure 5 Input and Output Characteristics PANI

Fabrication and Characterization PANI / ZnO Hybrid Nanocomposite based TFT

Fabrication of TFT on OHP sheet: The sheet is kept on a hot plate and heated to 75°C. The PANI/ZnO solution id drop-cast on to the heated substrate. The PANI/ZnO and OHP sheet acts as semiconductor and insulator material for the TFT. The silver paste act as a source, drain and gate electrode. The W/L ratio of the TFT is 2000/500 µm, as shown in Figure 6.

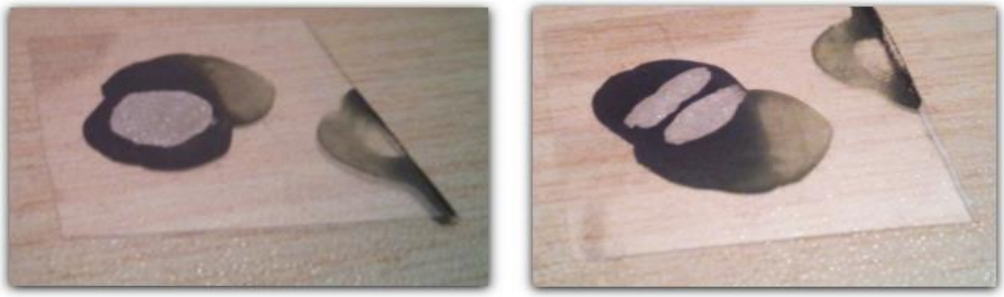


Figure 6 PANI / ZnO NC based TFT as-fabricated on OHP sheet

Characterization of TFT on OHP sheet*:* The Fabricated TFT is tested for its input and output characteristics. The Vth is determined to be 2.7 V, as shown in Figure 7. The value of μ_{lin} is found to be 3 X 10^{-5} cm/Vs. The Ion/off is in the range of 10^2, as shown in Figure 7.

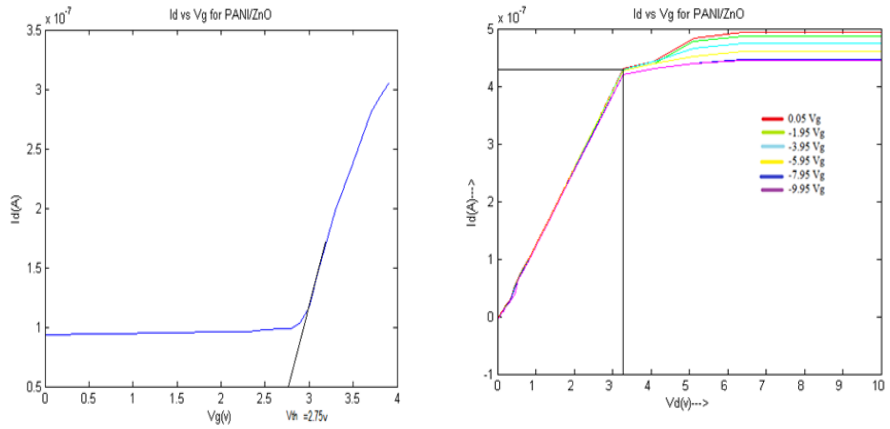


Figure 7 Input and output Characteristics of PANI / ZnO NC on the OHP Sheet

Fabrication of TFT on Glass: Top Gate-Top contact transistor is fabricated on the glass which is pre-coated with aluminium as a source and drain electrodes, PANI/ ZnO hybrid NC and PVA all using custom-designed masks. The PANI/ ZnO hybrid NC acts as an active layer, and PVA acts as a gate dielectric for the fabricated TFT, as shown in Figure 8.

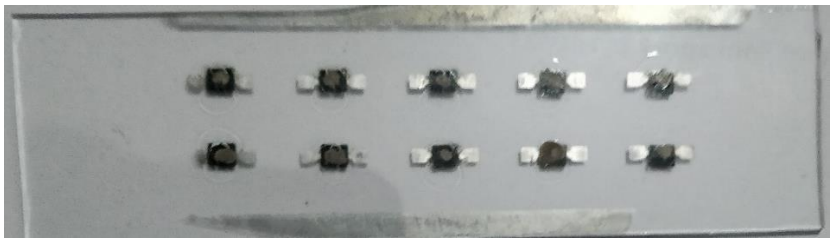


Figure 8 PANI / ZnO NC based TFT as-fabricated

Characterization of TFT on Glass*:* The Fabricated TFT is tested for its input and output characteristics. The Vth is determined to be 2.2 V, as shown in Figure 9. The value of μ_{lin} is found to be 3.8 X 10^{-4}. The Ion/off is in the range of 10^3, as shown in Figure 9.

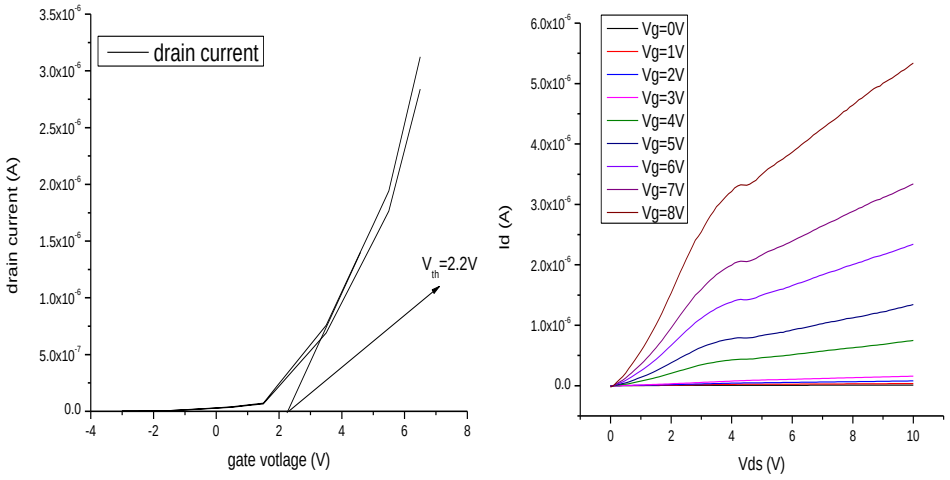


Figure 9 Input and output Characteristics of PANI / ZnO NC based TFT

Table 3 Results of PANI and PANI/ZnO hybrid TFTs

Substrate	W/L (µm)	Channel material	V_{th} in V	mobility ($cm^2 V^{-1} s^{-1}$)	$I_{on/off}$
Cellulose acetate	2000/130	PANI	4.3	$2X10^{-5}$	10^2
		PANI/ZnO hybrid Nanocomposite	2.7	$2.8X10^{-5}$	10^3
Glass	1000/200	PANI	3.7	$3X10^{-4}$	10^2
		PANI/ZnO hybrid nanocomposite	2.1	$3.8X10^{-4}$	10^3

Implementation of PANI / ZnO Hybrid Nanocomposite TFT as logic gates

Inverter (NOT gate): The fabricated inverter circuit is as shown in Figure 10. The inverter circuit is tested and obtained results are as shown in Table 4

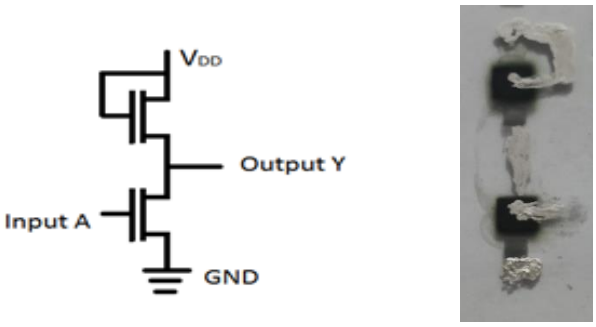


Figure 10 Inverter Circuit as fabricated on glass

Table 4 Truth Table of PANI/ZnO hybrid nanocomposite TFT based inverter

Input voltage	Input state	Output state	Output Voltage
0V	**0**	**1**	**4.5V**
5V	**1**	**0**	**1V**

NAND Gate: The fabricated NAND gate circuit is as shown in Figure 11 . The NAND gate circuit is tested and obtained results are as shown in Table 5

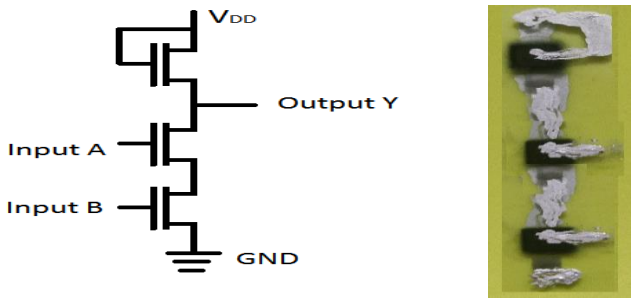


Figure 11 NAND Gate Circuit as fabricated on glass

Table 5 Truth Table of PANI/ZnO hybrid nanocomposite TFT based NAND gate.

Input A	Input B	Output Y	Output Voltage
0	0	1	3.3
0	1	1	3.3
1	0	1	3.3
1	1	0	1.4

NOR gate: The fabricated NOR gate circuit is as shown in Figure 12. The NOR gate circuit is tested and obtained results are as shown in Table 6

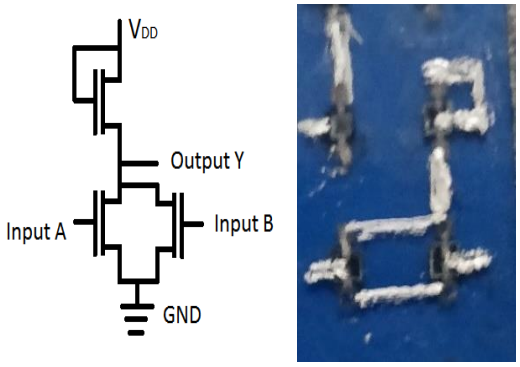


Figure 12 NOR Gate Circuit as fabricated on glass

Table 6 Truth Table of PANI/ZnO hybrid nanocomposite TFT based NOR gate.

Input A	Input B	Output Y	Output Voltage
0	0	0	1.4
0	1	0	1.3
1	0	0	1.3
1	1	1	3.4

Chapter 6; Synthesis Characterization and application of ZnO based TFT: In this chapter, we review the literature on oxide semiconductors and gate dielectrics. The synthesis of ZnO and PVA are explained. The deposition and characterization of these thin films are studied. The fabrication process is explained. The fabrication of TFT's on Teflon and glass slides are carried out. The TFT with various W/L ratio is fabricated and characterized. The TFT fabricated were used to construct and test the logic gates.

ZnO thin films: The thickness of the thin film is in the range of 440 to 470 nm. The roughness of the samples is between 160-170 nm. The XRD pattern confirms the amorphous nature of the film. EDAX endorses that the film is Zinc Oxide. The film exhibits the maximum transmission of 70% at 550 nm and the sharp ultraviolet edge is seen at 370 nm. The bandgap of the film was found to be 3.1 eV.

PVA film: The thickness is about 600 nm. It exhibits a maximum transmission of 90% at 550nm and the sharp ultraviolet edge is seen at 290 nm. The energy band gap is found to be 3.9 eV. The dielectric constant (εr) of the film is found to be 8 at 40 Hz.

Fabrication and characterization of ZnO based TFTon glass.

Fabrication of ZnO based TFTs on Glass: Top Gate-Top contact transistor is fabricated on the glass which is pre-coated with aluminium as a source and drain electrodes. The ZNO acts as an active layer and PVA acts as a gate dielectric for the fabricated TFT. The TFT were fabricated with different W/L ratio as shown in Figure 13.

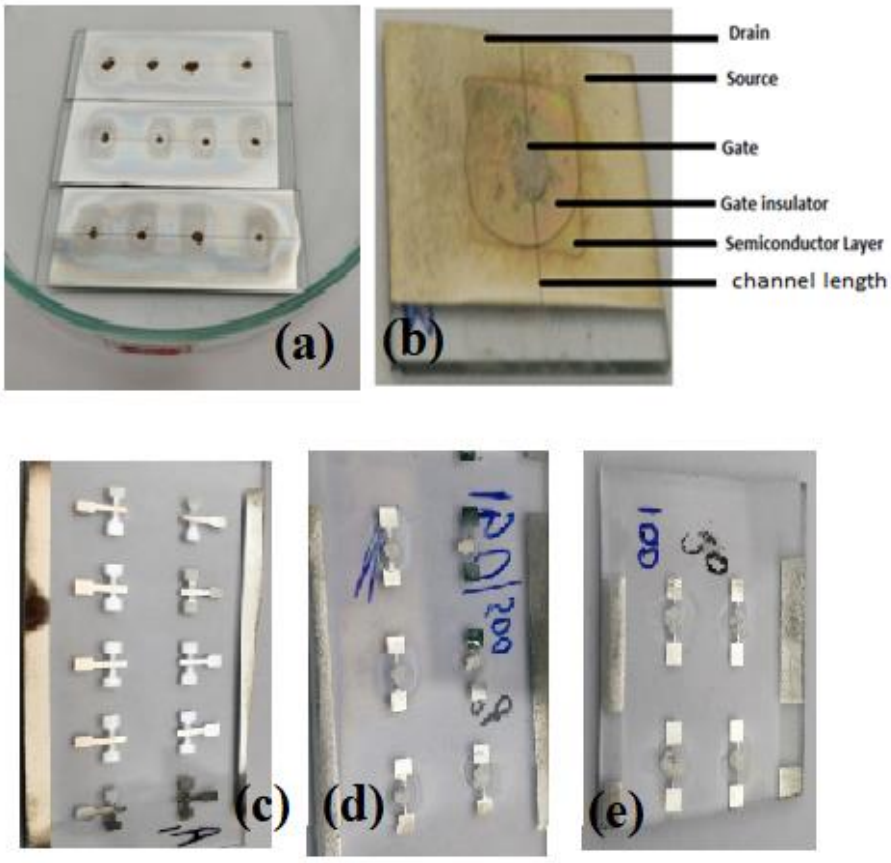


Figure 13 Images of Fabricated TFT on a Glass Substrate with Channel Length (b) 135 µm, (c)200 µm, (d)150 µm, e)100 µm

Characterization of TFT on Glass: The Fabricated TFT is tested for its input and output characteristics. The result of the TFT are shown Figure 14 Figure 15 Figure 16 Figure 17 tabulated in the Table 7.

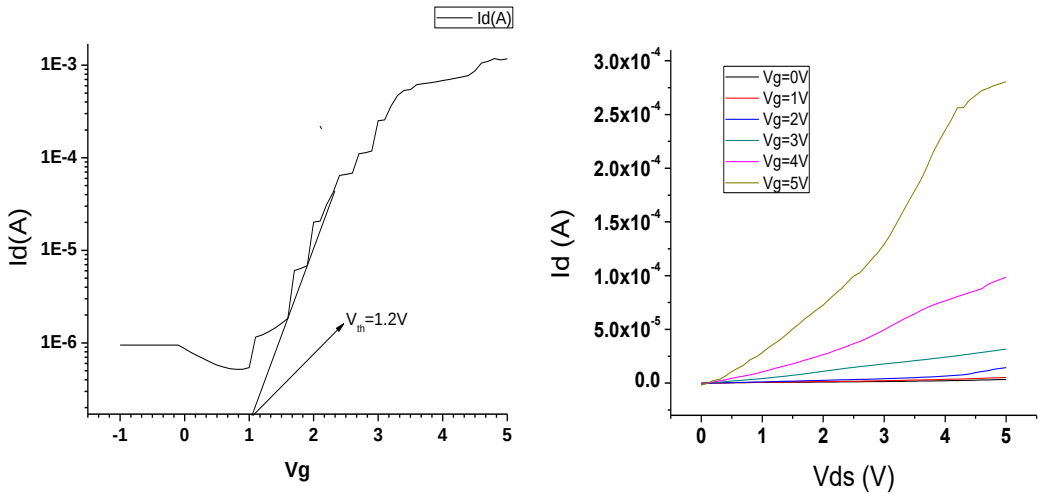


Figure 14 Input and Output Characteristics of TFT with W/L Ratio 2000/130 µm.

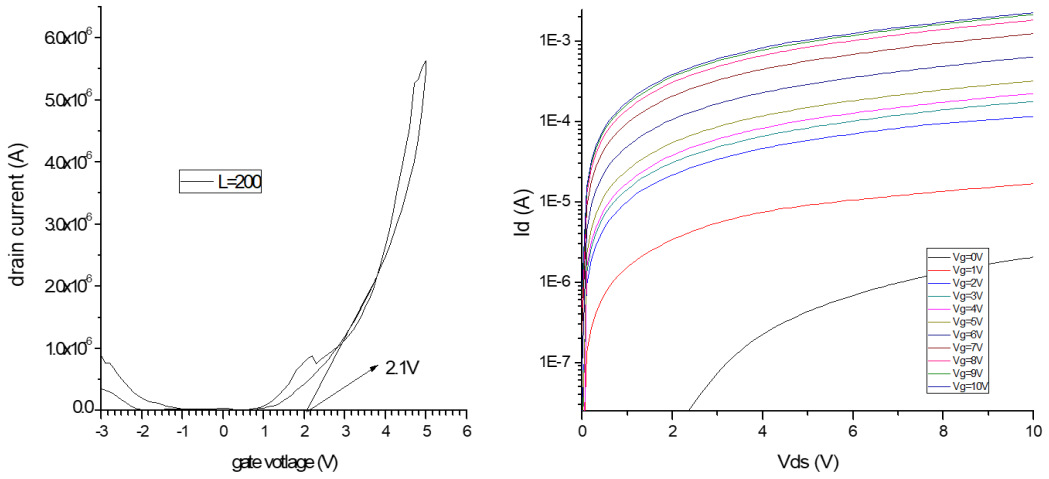


Figure 15 Input and Output Characteristics of TFT with W/L Ratio 1000/200 µm.

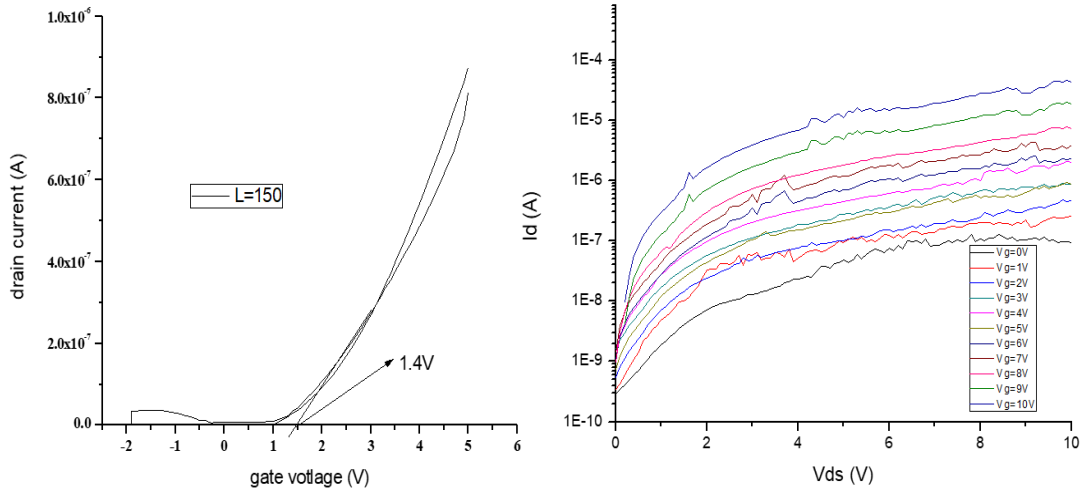


Figure 16 Input and Output Characteristics of TFT with W/L Ratio 500/150 µm

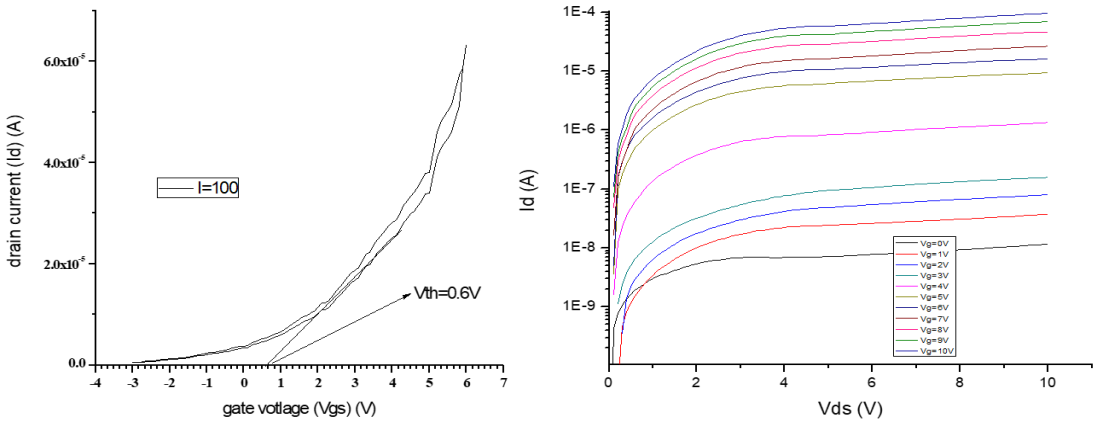


Figure 17 Input and Output Characteristics of TFT with W/L Ratio 500/100 µm

Table 7 Summary of the Result of Amorphous ZnO TFT

Sl no.	W/L in µm	V_{th} (in V)	Mobility ($cm^2 V^{-1} s^{-1}$)	$I_{(on/off)}$
1	2000/130	1.2	3.8	10^4
2	1000/200	2.1	4.8	10^4
3	500/150	1.4	4.1	10^3
4	500/100	0.6	5.8	10^5

Fabrication and characterization of ZnO based TFTon Teflon.

Fabrication of ZnO based TFTs on Teflon sheet: Top Gate-Top contact transistor is fabricated on the Teflon sheet which is pre-coated with aluminium as a source and drain electrodes. The ZNO acts as an active layer and PVA acts as a gate dielectric for the fabricated TFT. The TFT were fabricated with different W/L ratio as shown in Figure 18.

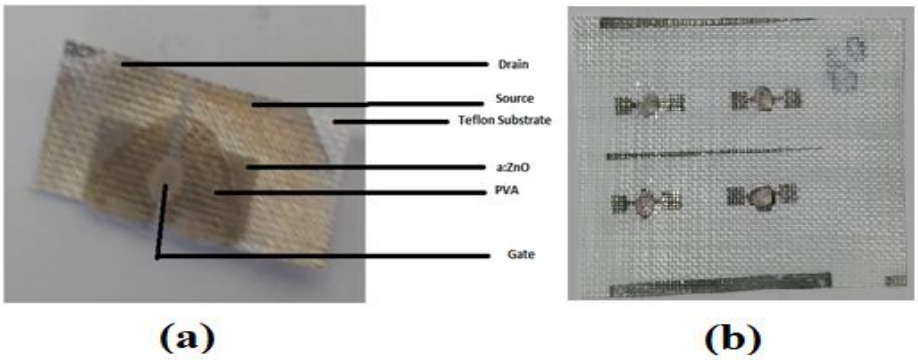


Figure 18 Images of TFT Fabricated on the Teflon Sheet as a Substrate with Channel Length (a) 135µm, (b) 100 µm

Characterization of TFT on Teflon sheet: The Fabricated TFT is tested for its input and output characteristics. The result of the TFT are shown in Figure 19 Figure-20. The TFTs were fabricated on Teflon substrates with different W/L ratios to measure Vth, mobility, and $I_{on/off}$ is as tabulated in Table 8.

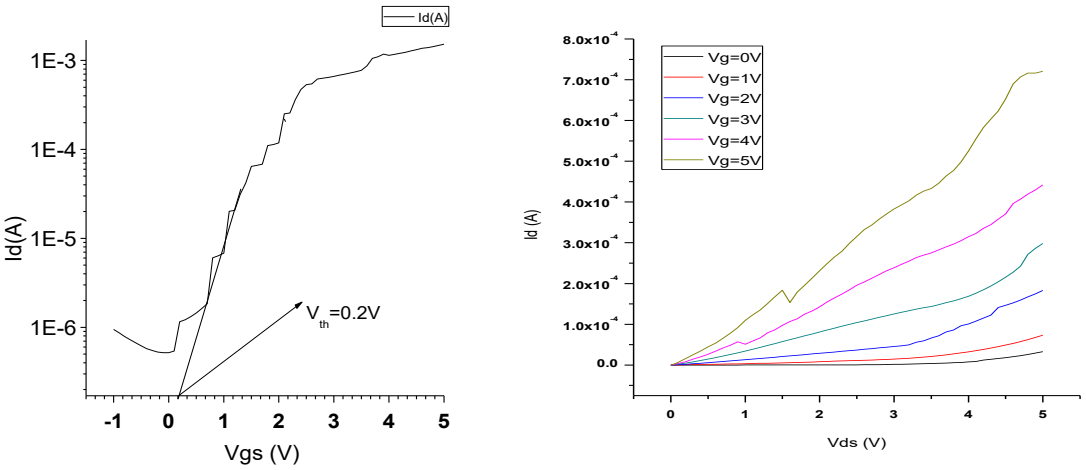


Figure 19 Input and Output Characteristics of TFT with W/L Ratio 2000/130 µm.

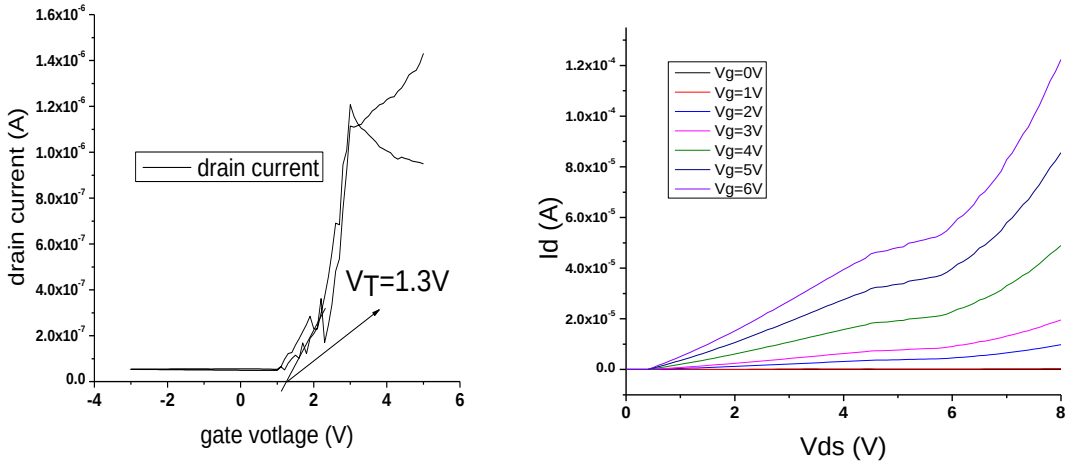


Figure-20 Input and Output Characteristics of TFT with W/L Ratio 500/100 µm

Table 8 Summary of the result of amorphous ZnO TFT

Sl no.	W/L in µm	V_{th} (in (V)	Mobility ($cm^2 V^{-1} s^{-1}$)	$I_{(on/off)}$
1	2000/130	0.2	2	10^3
2	500/100	1.3	2.4	10^4

Implementation of ZnO TFT as logic gates

Inverter (NOT gate): The fabricated inverter circuit is as shown in Figure 21 . The inverter circuit is tested and obtained results are as shown in Table 9.

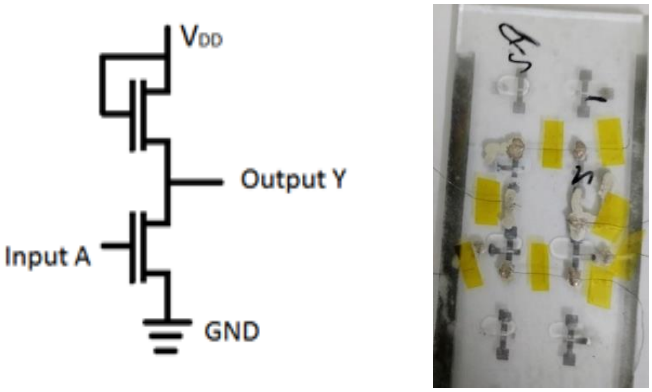


Figure 21 Inverter Circuit

Table 9 Truth Table of a-ZnO TFT based inverter

Input voltage	Input state	Output state	Output Voltage
0V	0	1	4.5V
5V	1	0	1V

NAND Gate: The fabricated NAND gate circuit is as shown in Figure 22. The NAND gate circuit is tested and obtained results are as shown in Table 10

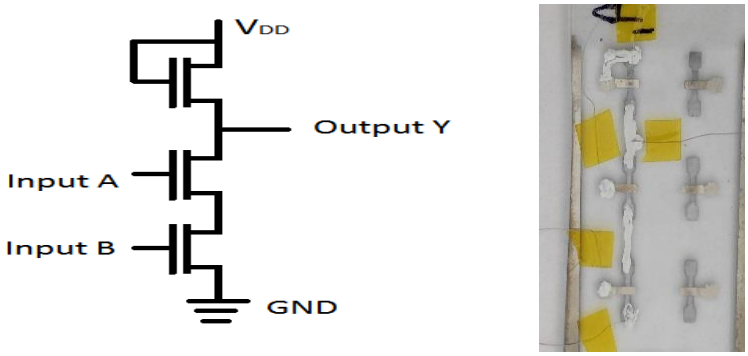
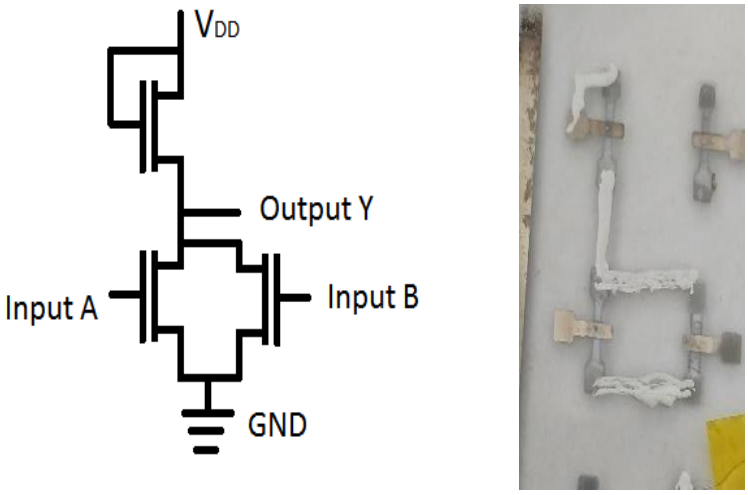


Figure 22 NAND Gate Circuit

Table 10 Truth Table of a-ZnO TFT based NAND gate.

Input A	Input B	Output Y	Output Voltage (in V)
0	0	1	7.7
0	1	1	7.6
1	0	1	7.9
1	1	0	1.9

NOR Gate: The fabricated NOR gate circuit is as shown in`Figure 23 . The NOR gate circuit is tested and obtained results are as shown in Table 11.



`Figure 23 NOR Gate Circuit

Table 11 Truth Table of a-ZnO TFT based NOR gate.

Input A	Input B	Output Y	Output Voltage
0	0	0	1.7
0	1	0	1.6
1	0	0	1.9
1	1	1	7.9

Chapter 7; Summary and future Work: The observed results of the SSP unit are summarized for different material coating. The characteristics of thin

film transistors fabricated using PANI, PANI/ZnO, and ZnO as an active layer are summarized. The result of the logic gates is discussed. The future scope of the work is to automate the SSP unit. The application transistor as the sensor is implemented.

1.3 Notable Outcomes of the Research Work

List of Journal

1. Omprakash S.S, Naveen Kumar S.K, Ravishankar Holla, "Titanium dioxide and Zinc oxide as a Dielectric Material for Application in TFT's," Materials Today: Proceedings 5 (2018) 10833–10838, 2018.

   https://doi.org/10.1016/j.matpr.2017.12.370

2. Omprakash S.S, Naveen Kumar S.K, "PANI/ZnO Hybrid Nanocomposites TFT for NAND Gate Application," Materials Today: Proceedings 5 (2018) 10827–10832, 2018.

   https://doi.org/10.1016/j.matpr.2017.12.369

3. Omprakash S.S, Naveen Kumar S.K, "Fabrication of Flexible Metal Oxide Thin Film Transistor by Indigenously Developed Spray Pyrolysis Unit," ECS Transactions 88(1):129-138, 2018.

   https://doi.org/10.1149/08801.0129ecst

4. Omprakash S.S, Naveen Kumar S.K, "Fabrication of Custom-Designed and Cost-Effective Spin-Spray Pyrolysis Unit," in International Journal of Engineering and Advance Technology, 2019.

   https://DOI:10.35940/ijeat.A1097.109119.

5. Omprakash S.S, Naveen Kumar S.K, "Solution Processed Amorphous Zinc Oxide Thin Film Transistor Based NAND Gate," in IOP Conf. Series: Journal of Physics: Conf. Series 1455 (2020) 012023

   https://doi:10.1088/1742-6596/1455/1/012023

6. Omprakash S.S, Naveen Kumar S.K, "Solution Processed Amorphous Zinc Oxide Thin Film Transistor Based Inverter," in AIP Conference Proceedings 1455 (2020) 012023

7. Naveen Kumar S.K, Vijaya Krishna, Omprakash S.S, "Structural, Electrical Characterization of PANI/ZnO Hybrid Nanocomposites TFT for Logic Gate Application," Proc. of the Intl. Conf. on Nanotechnology for Better Living, 2016 Vol. 3, No. 1, p. 22, 2016.

https://doi:10.3850/978-981-09-7519-7nbl16-rps-22

8. Omprakash S.S, Santhosh Kumar N, Naveen Kumar S.K, "Comparison of Aluminium with Copper for Better Contact on FTO Glass Substrate," Proc. of the Intl. Conf. on Nanotechnology for Better Living, 2016 (NBL-2016)Vol. 3, No. 1, p. 127, 2016.

https://doi:10.3850/978-981-09-7519-7nbl16-rps-127

List of Presented Papers in Conference

1. Omprakash S.S, Naveen Kumar S.K, "CNT Thin Film Transistor Based on Al2O3 High-K Dielectrics Deposited by Spray Pyrolysis in Air," in International Conference on Nanotechnology (ICNano-2016) held at VTU PG Center Muddenhalli, Chikkabalapur, Karnataka.

2. Omprakash S.S, Naveen Kumar S.K, "Structural, Electrical Characterization of PANI/ZnO Hybrid Nanocomposites TFT for Logic Gate Application," in 3rd International Conference on Nanotechnology for Better Living (ICBNL-2016) at NIT Srinagar, Jammu & Kashmir.

3. Omprakash S.S, Naveen Kumar S.K, "PANI/ZnO Hybrid Nanocomposites TFT for NAND Gate Application," Second International Conference on Large area and Flexible Microelectronics (ILAFM-2016) at R.V. College of Engineering Bangalore, Karnataka.

4. Omprakash S.S, Naveen Kumar S.K, "Titanium Oxide and Zinc Oxide as a Dielectric Material for Application in TFT's" Second International Conference on Large area and Flexible Microelectronics (ILAFM-2016) at R.V. College of Engineering Bangalore, Karnataka.

5. Omprakash S.S, Naveen Kumar S.K, “Study Of Amorphous Zinc Oxide Thin Film By Custom-Designed Low-Cost Spray Pyrolysis Unit,” Third International Conference on Nanomaterials: Synthesis, Characterization and Applications (*ICN 2018*) at Mahatma Gandhi University, Kottayam, Kerala.

6. Omprakash S.S, Naveen Kumar S.K, “Design And Fabrication Of Custom-Designed Low-Cost Spray Pyrolysis Unit,” Third International Conference on Nanomaterials: Synthesis, Characterization and Applications (*ICN 2018*) at Mahatma Gandhi University, Kottayam, Kerala.

7. Omprakash S.S, Naveen Kumar S.K, “Fabrication Of Flexible Metal Oxide Thin Film Transistor By Indigenously Developed Spray Pyrolysis Unit,” First International Conference on 4D Materials and Systems (4DMS) at Yamagata University, Yonezawa, JAPAN.

8. Omprakash S.S, Naveen Kumar S.K, “Solution Processed Amorphous Zinc Oxide Thin Film Transistor Based Inverter,” International Conference on Physics of Materials and Nanotechnology (ICPN 2019) at Mangalore University, Mangalore, Karnataka.

9. Omprakash S.S, Naveen Kumar S.K, “Solution Processed Amorphous Zinc Oxide Thin Film Transistor Based NAND gate,” 3rd International Conference on Recent Trends in Science, Engineering and Mathematics (ICRTSEM- 2019) at GOA, India.

List of Paper Communicated to Journals

1. Impact of Deposition Temperature on Amorphous Zinc Oxide Thin Film Characteristics to Spring Publication.
2. Fabrication of Amorphous ZnO TFT with Tunable Channel Length to Spring Publication.

1.4 Reference

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